What Is Claimed Is:

Sub A1

1. An apparatus for compressing video data, comprising:

a video input port, for receiving video data for a current video frame;

a video input buffer coupled to the video input port, for storing video data from the video input port;

a previous frame buffer, for storing at least a portion of a previous video frame;

an operation unit coupled to the video input buffer and the previous frame buffer, for performing an operation between data from the video input buffer and data from the previous frame buffer; and

a result buffer coupled to the operation unit, for storing the result of an operation from the operation unit.

Sub E2

2. The apparatus of claim 1, including a memory port coupled to the previous frame buffer and the result buffer, for transferring data to and from a memory that stores video data from the video input port and result data from the result buffer.

3. The apparatus of claim 2, including a memory coupled to the memory port for storing the video data from the video input port and result data from the result buffer, wherein the video data is stored to in a current frame area in the memory and the result data is stored in a difference frame area in the memory.

4. The apparatus of claim 3, wherein the memory stores a current video frame and a previous video frame in the same location in the memory, allowing the current video frame to be written over the previous video frame.

E2 cont'd

5. The apparatus of claim 3, wherein the memory also stores instructions and data for a central processing unit of a computer system.

6. The apparatus of claim 1, wherein the operation unit performs an exclusive-OR operation between data from the video input buffer and data from the previous frame buffer.

7. The apparatus of claim 1, wherein:

the video input buffer stores a block of data from the video input port;

the previous frame buffer stores a block of data from the previous video frame;

the result buffer stores a block of data from the operation unit; and

the operation unit performs an operation between a block of data from the video input port and a block of data from the previous frame buffer.

8. The apparatus of claim 1, wherein the apparatus resides inside of a core logic chip for a computer system.

9. The apparatus of claim 1, wherein the apparatus comprises part of a video conferencing system.

10. The apparatus of claim 1, including additional resources within the apparatus, for compressing the video data from the video input port.

11. The apparatus of claim 1, including a color space conversion circuit coupled between the video input port and the video input buffer.

12. The apparatus of claim 1, wherein the video input buffer is a register that stores less than one video frame.

13. An apparatus for compressing video data, comprising:

a video input port, for receiving video data for a current video frame;

a video input buffer coupled to the video input port, for storing video data from the video input port;

a previous frame buffer, for storing at least a portion of a previous video frame;

an exclusive-OR unit coupled to the video input buffer and the previous frame buffer, for performing an exclusive-OR operation between data from the video input buffer and data from the previous frame buffer;

a result buffer coupled to the operation unit, for storing the result of an operation from the operation unit;

a memory port coupled to the previous frame buffer and the result buffer, for transferring data to and from a memory that stores video data from the video input port and result data from the result buffer; and

a memory coupled to the memory port for storing the video data from the video input port and result data from the result buffer, wherein the video data is stored to in a current frame in the memory and the result data is stored in a difference frame in the memory.

14. The apparatus of claim 13, wherein the memory stores a current video frame and a previous video frame in the same location, allowing the current video frame to be written over the previous video frame.

15. The apparatus of claim 13, wherein the memory stores instructions and data for a central processing unit of a computer system.

16. The apparatus of claim 13, wherein:

the video input buffer stores a block of data from the video input port;

the previous frame buffer stores a block of data from the previous video frame;

the result buffer stores a block of data from the operation unit; and

the exclusive-OR unit performs an exclusive-OR operation between a block of data from the video input port and a block of data from the previous frame buffer.

17. The apparatus of claim 13, wherein the apparatus resides inside of a core logic chip for a computer system.

18. The apparatus of claim 13, wherein the apparatus comprises part of a video conferencing system.

19. The apparatus of claim 13, including a color space conversion circuit coupled between the video input port and the video input buffer.

20. A computer system including resources for compressing video, comprising:

a central processing unit within the computer system;

a video input port, for receiving video data for a current video frame;

a video input buffer coupled to the video input port, for storing video data from the video input port;

a previous frame buffer, for storing at least a portion of a previous video frame;

an operation unit coupled to the video input buffer and the previous frame buffer, for performing an operation between data from the video input buffer and data from the previous frame buffer; and

a result buffer coupled to the operation unit, for storing the result of an operation from the operation unit.

A3 cont'd